UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,273	09/18/2003	Kerim Kalafala	FIS920030267US1	5468

7590 10/12/2005	EXAMINER
H. Daniel Schnurmann	TAT, BINH C

Intellectual Property Law	ART UNIT / PAPER NUMBER
IBM Corporation, Dept. 18G	
Building 300-482, 2070 Route 52	2825
Hopewell Junction, NY 12533	

DATE MAILED: 10/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/665,273	KALAFALA ET AL.
	Examiner	Art Unit	
	Binh C. Tat	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>18 September 2003</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-30</u> is/are pending in the application.

     4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-30</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>14 October 2004</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

     a)☐ All   b)☐ Some *   c)☐ None of:

         1.☐ Certified copies of the priority documents have been received.

         2.☐ Certified copies of the priority documents have been received in Application No. _____.

         3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

     * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
     Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
     Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1.   This office action is in response to application 10/665273 file on 09/18/03.

Claim 1-30 remain pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2.   Claims 1-30 are rejected under 35 U.S.C. 102(e) as being anticipated by You et al. (US

Patent 6799308).

3.   As to claims 1, 26, and 30 You et al. teach a method for performing static timing analysis

of a digital system in the presence of a plurality of global sources of delay variation comprising

the steps of: a) selecting, for at least one timing test, at least one pair of an early path and a late

path leading to said timing test (see fig 4b col 6 lines 8-55); b) identifying at least one global

parameter which the delays of said early and late paths depend on (see fig 4a, 4b col 4 lines 48 to

col 6 line 55); c) determining for at least one of said global parameters at least one consistent

value assignment (see fig 6-10 col 8 lines 48 to col 13 lines 54 especially col 13 lines 22-30); and

d) computing for each said consistent assignment a slack value for said path pair (see fig 6-10 col

8 lines 48 to col 13 lines 54 especially col 11 lines to col 12 lines 47).

4.   As to claim 2, You et al. teach wherein one of said early and late paths is a clock path and

the other of said early and late paths is a data path (see fig 4b col 6 lines 8-55 and background).

5.   As to claim 3, You et al. teach wherein said at least one timing test comprises those

timing tests within said digital system whose slack falls below a specified threshold after an

initial static timing analysis (see fig 6-10 col 8 lines 48 to col 13 lines 54 especially col 11 lines

to col 12 lines 47).

6.   As to claim 4, You et al. teach wherein said identified path pair comprises a late critical

path to said timing test and an early critical path to said timing test (see fig 4a-4b col 5 lines 39-

to 6 lines 41).

7.   As to claim 5, You et al. teach wherein said initial static timing analysis is performed

using bounding parameter values (see fig 6-10 col 8 lines 48 to col 13 lines 54 especially col 13

lines 22-30).

8.   As to claim 6, You et al. teach further comprising the step of determining for each of said

timing tests the worst of said computed slacks (see fig 4a-4b col 5 lines 39- to 6 lines 41 and

summary).

9.   As to claim 7, and 27 You et al. teach wherein said step c) further comprises the steps of:

e) enumerating combinations of realizable values of at least one of said identified parameters

(see fig 6-10 col 8 lines 48 to col 13 lines 54 especially col 13 lines 22-30); and f) performing a

timing analysis for each of said enumerated combinations (see fig 6-10 col 8 lines 48 to col 13

lines 54 especially col 13 lines 22-30).

10.   As to claim 8, You et al. teach wherein said step e) is terminated after one of the timing analyses of step t) produces a slack below a specified threshold (see fig 6-10 col 8 lines 48 to col 13 lines 54 especially col 13 lines 22-30).

11.   As to claim 9, You et al. teach wherein at least one parameter whose realizable values are enumerated comprises a subset of the parameters identified in step b) (see fig 4a, 4b col 4 lines 48 to col 6 line 55).

12.   As to claim 10, You et al. teach wherein said step e) is repeatedly applied to additional ones of said identified parameters until said step t) results in a slack which is geater than a specified slack threshold (see fig 6-10 col 8 lines 48 to col 13 lines 54 especially col 13 lines 22-30).

13.   As to claim 11 and 28, You et al. teach wherein said step b) further comprises identifying parameters in which delay functions are separable, and said step c) further comprises setting independently each of said parameters in which delay functions are separable to the value that results in the worst slack value at said timing test (see fig 6-10 col 8 lines 48 to col 13 lines 54 especially col 13 lines 22-30).

14.   As to claim 12, and 29 You et al. teach wherein said step of independently setting parameter values further comprises the steps of: e) summing along the early and late paths of said path pair sensitivities of delay elements with respect to each of said parameters in which delay functions are separable (see fig4a-4b col 4 lines 48 to col 6 lines 55); t) computing the difference between said summed path sensitivities of said early and late paths, and g) determining a value of each of said parameters in which delay functions are separable according

to an arithmetic sir of said difference of sensitivities (see fig 6-10 col 8 lines 48 to col 13 lines 54 especially col 13 lines 22-30).

15.   As to claim 13, You et al. teach further comprising the step of determining whether the slack of any other early and late path pair to said timing test is worse than said determined worst slack, and if so, repeating said steps b), c), and d) for said other path pair (see fig 6-10 col 8 lines 48 to col 13 lines 54 especially col 13 lines 22-30 and summary).

16.   As to claim 14, You et al. teach wherein the timing analysis is performed at a gate- level (see fig 4-6 col 4 lines 48 to col 6 lines 55 and background).

17.   As to claim 15, You et al. teach wherein the timing analysis is performed at a transistor- level (see fig 4-6 col 4 lines 48 to col 6 lines 55 and background).

18.   As to claim 16, You et al. teach wherein the delay models are stored as pre- determined tables (see fig 4-6 col 4 lines 48 to col 6 lines 55 and background).

19.   As to claim 17, You et al. teach wherein the delay models are stored as pre- determined analytic equations (see fig 4-6 col 4 lines 48 to col 6 lines 55 and background).

20.   As to claim 18, You et al. teach wherein the delay models are computed on the fly (see fig 4-6 col 4 lines 48 to col 6 lines 55 and background).

21.   As to claim 19, You et al. teach wherein the circuit comprises a plurality of clock domains (see fig 7-8 col 9 lines 29 to col 10 lines 11).

22.   As to claim 20, You et al. teach wherein the circuit is selected from the group consisting of at least one of the following clock configurations: mesh network, tree network, hybrid network, gated clocks and pulsed clocks (see fig 7-9 col 9 lines 29 to col 10 lines 66).

23.   As to claim 21, You et al. teach wherein the sources of variability include a mistrack

between one or more of the following device families that is selected from the group consisting

of devices having different threshold voltages, devices having different gate oxide thicknesses

and devices having different characteristics for PFET and NFET devices (see fig 1a-c col1 lines

30-65).

24.   As to claim 22, You et al. teach wherein the sequential elements are selected from the

group consisting of at least one of: master-slave latches, flip-flops, edge-triggered latches, level-

sensitive latches and transparent latches (see fig 7-9 col 9 lines 29 to col 10 lines 66).

25.   As to claim 23, You et al. teach wherein the timing analysis is conducted for timing

verification at one or more levels selected from the group consisting of a circuit level, macro

level, functional-unit level, chip level, board level and system level (see fig 7-9 col 9 lines 29 to

col 10 lines 66 and background).

26.   As to claim 24, You et al. teach wherein the circuit being analyzed is selected from the

group consisting of at least one of the following technologies: CMOS, domino, static logic and

dynamic logic (see fig 4-6 col 4 lines 48 to col 6 lines 55 and background).

27.   As to claim 25, You et al. teach wherein the global sources of variation include one or

more of manufacturing variations, device fatigue variations, environmental variations, modeling

variations, and circuit operation variations (see fig 4-6 col 4 lines 48 to col 6 lines 55 and

background).

Conclusion

28.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is (571) 272-1908. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew Smith can be reached on (571) 272-1907. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-1908 for regular communications and (703) 305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Binh Tat
Art unit 2825
October 5, 2005